REMARKS

The Applicant thanks the Examiner for the prompt and thorough Office Action dated December 19, 2002. Applicant has amended claim 6 to overcome the objection raised on page 2 of the Office Action.

The Examiner rejected claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by *Gates*. The *Gates* publication discloses an etch stop layer 56 interposed between the dielectric layers 54, 58. *Gates* utilizes a dual damascene method demonstrated in FIGs. 5-8 for the fabrication of an interconnect structure, including the formation of a opening (trench) 66 and a second opening (via) 68 in the hard mask 60. As explained in more detail on page 4, beginning with paragraph 49, line 1, the trench 66 is first etched into the layer 64'. A new photoresist is applied to the structure and subject to lithograph and etching so as to provide the second opening 68 in the structure which exposes a surface of cured multilayer of spun on dielectrics 52'. See, page 4, para. 51. As set forth on page 4, paragraph 51, following the second etch (*i.e.*, the via etch) "which exposes the cured multi-layer of spun-on dielectrics, the second photoresist is stripped from the structure utilizing a conventional stripping process, providing a structure shown as in FIG. 6." Accordingly, etching the via exposes the underlying dielectric material 58.

Amended claim 1 includes the limitation of "forming a via in the mask <u>without exposing the underlying dielectric material</u>, . . . then forming a trench in the mask layer which is not as deep as said first predetermined depth of the via formed in the mask layer . . ." (emphasis added). A via is thereby etched in the mask layer without exposing the underlying dielectric material, which limitation is not disclosed in *Gates*. Moreover, in the amended claim 1, the via is formed in the mask layer before the trench is formed in the mask layer.

The Examiner rejected independent claim 6 under 35 U.S.C. §103(a) as unpatentable over *Gates* in view of the *Gutsche* reference. The *Gutsche* reference discloses a method of fabricating a semiconductor device that includes the formation of a mask layer having "*n*" mask films over three mask films. In FIGs. 1-2e, films 0, 1, 2, 3

of the mask layers are selectively etched to form a feature. The *Gutsche* reference discloses a single damascene method of fabrication as opposed to a dual damascene method of fabricating interconnect structures set forth in claim 1, 6 and 18. Accordingly, *Gutsche* discloses a damascene material that etches only a single feature into the mask layer and transfers the feature to the underlying dielectric material.

A combination of *Gates* and *Gutsche* would, at most, discloses the use of a dual damascene process shown in *Gates*, by which a trench is first etched into a mask layer, and then a via is subsequently etched, exposing the underlying dielectric material. Etching the via in such a "partial trench first" fabrication method exposes the low-k dielectric to photoresist material used to pattern the via. Given the porosity of the low-k dielectric material, the photoresist will damage the low-k dielectric, which damage affects the integrity of the conductive lines and/or interconnections formed within the semiconductor device.

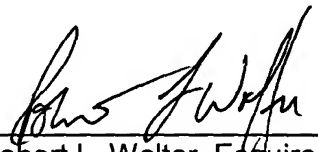
Accordingly, with respect to claim 6, neither *Gates* nor *Gutsche* disclose all the elements of claim 6, nor would it have been obvious to combine *Gates* and *Gutsche* to arrive at an invention having the limitations of claim 6. Claim 18 contains limitations similar to the amended claim 6, and is allowable for the above stated reasons.

Applicant directs the Examiner's attention to the Supplemental Information Disclosure Statement, and more specifically, to Chan, *et al.,* U.S. Patent No. 6,312,874 B1. The *Chan* patent discloses a dual damascene method of forming an interconnect structure. As shown in FIG. 3a, *Chan* utilizes a mask layer 58 composed of three films 52, 54 and 56. As further depicted in FIGs. 3a through 3c, and explained in more detail in column 5 and column 6, lines 1 through 4, *Chan* selectively etches a trench through film 56 before selectively etching the via down to the film 52. Chan does not teach or suggest etching a via in the mask layer before etching the trench without exposing the underlying dielectric.

Applicant respectfully requests reconsideration of claims 1-22, as amended.

If further prosecution of this application can be facilitated via telephone conference, the Examining Attorney is invited to contact the undersigned at (407) 926-7706.

Respectfully submitted,



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I hereby certify that a true and correct copy of the above and foregoing Amendment was furnished by First Class Mail to the Commissioner of Patents, Box Non-Fee Amendment, Washington, DC 20231, this 17th day of March, 2003.

Gwendolyn C. Ramsey